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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/977,459	10/16/2001	Katsunori Hirase	011386	3658	
23850	7590 03/29/2004		EXAMINER		
	ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP			NATNAEL, PAULOS M	
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00	ON, DC 20006	2614	4		
			DATE MAILED: 03/29/2004	•	

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)				
	09/977,459	HIRASE ET AL.				
Office Action Summary	Examiner	Art Unit				
	Paulos M. Natnael	2614				
The MAILING DATE of this communicate Period for Reply	ation appears on the cover sheet wit	th the correspondence address				
A SHORTENED STATUTORY PERIOD FOR THE MAILING DATE OF THIS COMMUNIC. - Extensions of time may be available under the provisions of after SIX (6) MONTHS from the mailing date of this commun. - If the period for reply specified above is less than thirty (30) of the period for reply is specified above, the maximum statut. - Failure to reply within the set or extended period for reply will Any reply received by the Office later than three months after earned patent term adjustment. See 37 CFR 1.704(b).	ATION. 37 CFR 1.136(a). In no event, however, may a reication. days, a reply within the statutory minimum of thirty tory period will apply and will expire SIX (6) MON I, by statute, cause the application to become ABA	eply be timely filed y (30) days will be considered timely. THS from the mailing date of this communication. ANDONED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed	on <u>10/16/01</u> .					
)⊠ This action is non-final.					
3) Since this application is in condition fo	' _					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) ⊠ Claim(s) 1-17 is/are pending in the app 4a) Of the above claim(s) is/are 5) ⊠ Claim(s) 6-9 and 15-17 is/are allowed. 6) ⊠ Claim(s) 1,2 and 10-14 is/are rejected. 7) ⊠ Claim(s) 3-5 is/are objected to. 8) □ Claim(s) are subject to restriction	withdrawn from consideration.					
Application Papers						
9)☐ The specification is objected to by the 8	Examiner.	•				
10) The drawing(s) filed on is/are: a	10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.					
Applicant may not request that any objection	on to the drawing(s) be held in abeyan	ce. See 37 CFR 1.85(a).				
Replacement drawing sheet(s) including the	· ·					
11)☐ The oath or declaration is objected to b	by the Examiner. Note the attached	Office Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for a) All b) Some * c) None of: 1. Certified copies of the priority do 2. Certified copies of the priority do 3. Copies of the certified copies of application from the International	ocuments have been received. Ocuments have been received in Ap the priority documents have been all Bureau (PCT Rule 17.2(a)).	pplication No received in this National Stage				
Attachmont(a)						
Attachment(s) 1) X Notice of References Cited (PTO-892)	4) \prod Interview S	ummary (PTO-413)				
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTC 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PT Paper No(s)/Mail Date <u>3</u> .)-948) Paper No(s)/Mail Date formal Patent Application (PTO-152)				

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DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed limitation in claim **9**, "a scaling circuit scaling the image data supplied from said second weighting factor multiplier circuit according to respective resolutions of said plurality of image display units" and in claim **10**, the claimed "decoding unit reproducing said first and second image data from the output of said separating unit," must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:
 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims **10-14** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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In claim 10, the claimed phrase, "said multiplied second image data" lacks antecedent basis.

Claim 11-14 are rejected for being dependent on the rejected claim 10.

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 5. Claims **1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mills, US. Patent No. 5, 953,691.

Considering claim 1, Mills discloses the following claimed subject matter, note;

a) a first image data processing circuit scaling said first image data..., is met by alpha

pre-scaler 112 which scales the YUV signals using the weighting factor or alpha input to
the pre-scaler 112 from outside source. (fig. 3A) (see also col. 15, lines 2-32)

b) a second image data processing circuit weighting said second image data..., is met by Multiplier 118 which receive the alpha_i signal from the interpolator 114 and the Video signal input from outside source to it, the "interpolated blending value scales the decoded video signal in multiplier 118..." (col. 15, lines 35-37)

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c) a first combining circuit combining said first image data processed by said first Image data processing circuit and said second image data processed by said second image data processing circuit, is met by adder 116, fig. 3A which adds the alpha blended YUV signal and the alpha-blended video signal output from the interpolator 114, and outputs the combined video and graphics signal.

Except for;

- d) the claimed "and thereafter weighting said scaled first image data";
- e) the claimed "and thereafter scaling said weighted second image data";

Regarding d), the prescaler 112 blends the YUV signal with the alpha_0 signal and it also obviously scales the signal as evidenced by the name: prescaler. However, Mills does not specifically disclose which process precedes the other one, which may mean that Mills does not consider the order of processing important one way or the other, since the processes may not be performed simultaneously, i.e., at exactly the same time. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Mills so that the signal is first scaled then weighted, since Mills does not appear to consider or attach much importance which process comes first.

Regarding e), the Multiplier 118 multiplies the interpolated alpha_I with the video signal (v), and Mills discloses that "the interpolated blending value scales the decoded video signal in multiplier 118." (col. 15, lines 35-39) However, as also shown above in part (e), Mills does not specifically disclose which process precedes the other one.

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Again it appears that Mills does not consider the processing order important as such one way or the other, since the processes may not be performed exactly simultaneously one may come first and the other would follow almost instantly. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Mills so that the signal is first weighted and then scaled, since Mills, by not disclosing one way or the other, does not appear to attach any further importance which process comes first, i.e., whether one process precedes the other or vice versa.

Considering claim 2, the image data output device according to claim 1, wherein a weighting factor used by said first image data processing circuit is scaled according to resolution of an image display unit.

Regarding claim **2**, Mills discloses that "The set top box processor 20 includes a graphics processor 60 which can be configured to support a variety of graphics modes and resolutions...The graphics plane may be arranged to support multiple resolutions of pixel size and aspect ratio, including square pixels, multiple color modes, and multiple levels of alpha blending" (col. 12, lines 22-30) Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Mills by providing the method of scaling the weighting factor according to display resolution, so that the set top box processor 20 would be able to scale the signals according to the variety of display resolutions that it is configured to support.

6. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al., U.S. Patent No. 6,493,038 in view of Mills, US. Patent No. 5, 953,691.

Considering claim **10**, Singh et al discloses the following claimed subject matter, note; a) a tuner selectively receiving a signal transmitting first image data representing a moving image and second image data representing an image including characters and graphics, is met by Hybrid Tuner 51, fig.5; (see also col. 3, lines 45-64)

- b) a separating unit separating the received signal into a signal corresponding to said first image data and a signal corresponding to said second image data, is met by Philips Media Processor 53, fig.5, which is configured "to separate out and decode the video stream." (col. 3, lines 56-57)
- c) a decoding unit reproducing said first and second image data from an output of said separating unit, is also met by Philips Media Processor 53, fig.5, which is configured "to separate out and decode the video stream." (col. 3, lines 56-57)
- d) an image data output device receiving said first and second image data from said decoding unit to output an image signal corresponding to a composite image generated by combining said first and second data, is met by PIP Module 60, fig.5, which receives

the video out (YUV) and Graphics Out (YUV) signals from the processor 53 and outputs YUV PIP Out signal to DENC 66.

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Except for;

e) said image data output device including a first image data processing circuit scaling said first image data and thereafter weighting said scaled first image data, a second image data processing circuit weighting said second image data and thereafter scaling said multiplied second image data, and a first combining circuit combining said first image data processed by said first image data processing circuit and said second image data processed by said second image data processing circuit.

Regarding e), Singh discloses that both the decoded graphics out (YUV) and video out (YUV), output from the processor 53 are input to the PIP module 60. Singh also discloses that "... The image created by a PIP module is composed of a main part that occupies the full dimensions of the image, and one or more PIP parts that are scaled to occupy only a small portion of the overall image. The PIP part is typically wholly contained within the main part of the image." (col. 1, lines 17-24) Fig.3 of Singh shows the PIP module 10 receiving video sources 2 and 3 and blending the two signals in video blender 14 as shown in 15. Singh further teaches that "Video at the input to the PIP DSP 65 from demodulator 63 is scaled to 1/16 or 1/9 of its original size and multiplexed with the YUV signal from the Philips Media Processor 53." (col. 4, 32,-35) While teaching method of scaling, however, Singh does not disclose the details of such a scaler.

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Mills discloses a processing system with graphics data prescaling and, in fig.3A, teaches a Multiplier 118 for multiplying the alpha_I with the video signal (v). Mills further discloses that "the interpolated blending value scales the decoded video signal in multiplier 118." (col. 15, lies 35-39) Mills however does not specifically disclose which process precedes the other one, and it appears that Mills does not consider it important one way or the other. Since the processes may not be performed exactly simultaneously, one may come first and the other may follow almost instantly. It would have been therefore obvious to the skilled in the art at the time the invention was made to modify the system of Singh by providing the scaling and weighting circuit of Mills so that the signal is weighted and then scaled, or visa versa as desired, and output a desired size of video signal including graphics to a display device or for further processing.

Considering claim **11**, the receiving device according to claim 10, wherein a weighting factor used by said first image data processing circuit is scaled according to resolution of an image display unit.

Regarding claim 11, see rejection of claim 10 as modified above and claim 2.

Allowable Subject Matter

7. Claims **6-9** and **15-17** are allowable over the prior art.

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- 8. Claims **3-5** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
- 9. Claims **12-14** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
- The following is a statement of reasons for the indication of allowable subject 10. matter: the prior art fails to disclose an image data output device, wherein said first image data processing circuit includes first scaling circuit scaling said first image data and weighting factor multiplier circuit weighting said first image data scaled by said first scaling circuit, said second image data processing circuit includes a second combining circuit receiving said second image data for weighting at least one image data constituting said second image data and combining the weighted image data to generate one composite image data and a second scaling circuit scaling the composite image data generated by said second combining circuit, and said first combining circuit combines the image data supplied from said weighting factor multiplier circuit and the image data supplied from said second scaling circuit, as in claim 3; a plurality of first scaling circuits scaling said first image data according to respective resolutions of said plurality of image display units; a plurality of weighting factor multiplier circuits multiplying said first image data scaled by said plurality of first scaling circuits by respective weighting factors; a first combining circuit receiving said second image data

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for weighting at least one image data constituting said second image data and combining the weighted image data to generate one composite image data; a second scaling circuit scaling the composite image data generated by said first combining circuit according to respective resolutions of said plurality of image display units; and a plurality of second combining circuits combining image data supplied respectively from said plurality of weighting factor multiplier circuits and image data supplied from said second scaling circuit to generate and output composite image data according to respective resolutions of said plurality of image display units, as in claim 6; a plurality of first weighting factor multiplier circuits respectively multiplying, by respective weighting factors, first image data to be output respectively for said plurality of image display units and representing a moving image; a second weighting, factor multiplier circuit multiplying second image data representing an image including characters and graphics by a weighting factor; a scaling circuit scaling the image data supplied from said second weighting factor multiplier circuit according to respective resolutions of said plurality of image display units; and a plurality of combining circuits combining image data supplied respectively from said plurality of first weighting factor multiplier circuits and image data supplied from said scaling circuit to generate and output composite image data according to respective resolutions of said plurality of image display units, as in claims 9 and 15;

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Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Glen, U. S. Patent No. 6,310,659 discloses a graphics processing device and method with graphics versus video color space conversion discrimination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN March 17, 2004